AN ON-CHIP LOW POWER CLOCK MULTIPLIER UNIT IN 0.25 MICRON TECHNOLOGY

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Abstract

A new method to obtain a high frequency clock (1 GHz) from a low frequency reference clock (10 MHz) is presented in this paper. High frequency is achieved using two level sensitive flip-flops. Variable delay lines are used to ensure that the multiplied clock is running in correct frequency. In the newly designed multiplier, the low frequency reference clock itself at every of its falling and rising edge keeps the generated high frequency clock in phase. The clock multiplication is achieved with 82ps peak-to-peak jitter when the generated clock is 1 GHz and consuming 0.822mW power from 2.5 volt power supply. The performance of the multiplication unit is tested on PSPICE using BSIM3v3 model parameters in .25µm CMOS technology.

Keywords*: Delay-controlled oscillator, clock generator, voltage controlled delay line, frequency multiplication, low skew.*

1 Introduction

As systems are becoming faster and the dimension of the devices are becoming smaller, high frequency clocking is still a key issue in today's VLSI. At high frequencies, the distribution of clock signals throughout an entire system as well as with maintaining a low clock skew is a significant design problem. At chip level, the clock distribution in high frequency is more problematic because the wires are slow and lossy RC lines and the number of loads is large (10^4-10^5) compared to the off-chip network and skew gets easily too large. This creates the necessity of on-chip clock frequency multiplier.

In literature, several methods are described for high frequency clock generation from low input reference. One most commonly used way is to use voltage-controlled oscillator (VCO) with phase-locked loop (PLL) [1]-[3]. But this type of clock has some inherent problems [4], [5]. PLL is a higher order system and its locking time is larger. Moreover jitter accumulates over many cycles of time because the oscillation frequency of VCO may change due to power supply variation, substrate noise and process variation [6]. Recently digital phase locked loop has been used for clock frequency multiplication [7]. But the use of digital approach will obviously create quantization error [5]. As crystal resonator can produce frequency of several tens of megahertz, we can generate higher frequencies from its output [8]. But this clock contains harmonics and we need to use LC filter circuits to remove this [9]. But this type of filter will occupy most of the chip area and not utilitarian for on-chip clock multiplication.

Third method is delay-locked looped (DLL) based clock generators. They have several advantages compare to PLL based clock generators. DLL is a first order system, stable and easier to design [4]. One of the main advantages is that jitter does not accumulate over clock cycles. Several papers described DLL based clock frequency multiplier [4], [5]. In [5], a counter is used which occupies a large chip area and the size of the counter increases with the increase of multiplying factor. In this paper, we propose a new DLL-based clock generator which generates less jitter, consumes low power than the other clock generator. The main part of the clock generator is a delay-controlled oscillator. The oscillation is controlled using voltage-controlled delay line (VCDL). Our objective is to design an on-chip clock multiplier which will generate a high frequency from a low reference clock with a lower peak-to-peak jitter and generated clock will be in phase with the reference clock (minimum skew) consuming less power.

2 Architecture and Operational principle

2.1 System Overview

Fig. 1 shows the schematic diagram of the proposed clock frequency multiplier. It constitutes of four main blocks: delay controlled oscillator (level sensitive flip-flop), voltage controlled delay line (VCDL), delay controller and charge pump. The frequency of oscillation of the delay controlled oscillator is controlled by the VCDL. Delay controller is a phase detector (PD) whose output is proportional to the phase relation between the inverted reference clock and generated clock. The operation principle of the clock generator has been described in the following sections.

2.2 The Level sensitive Flip-flop

The schematic of a conventional level sensitive flip-flop is shown in fig. 2. This level sensitive flip-flop with a delay line

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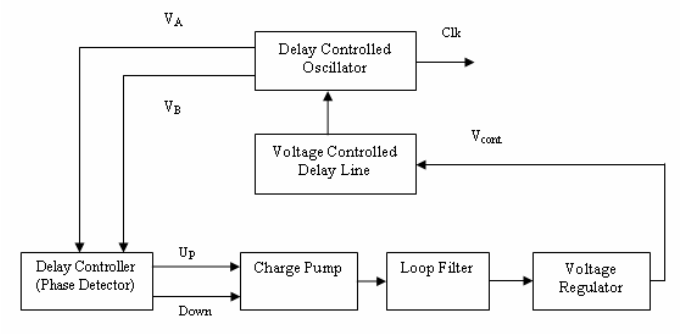

Fig. 1. Block diagram of the proposed DLL based clock generator

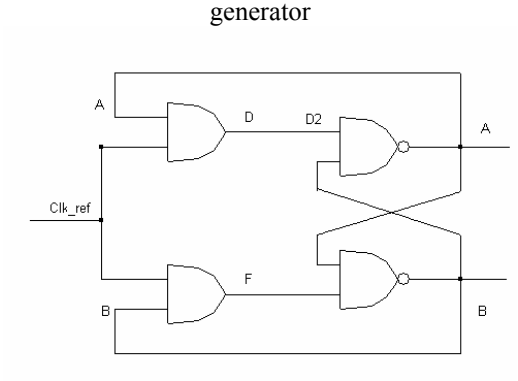

Fig. 2. The level sensitive flip-flop

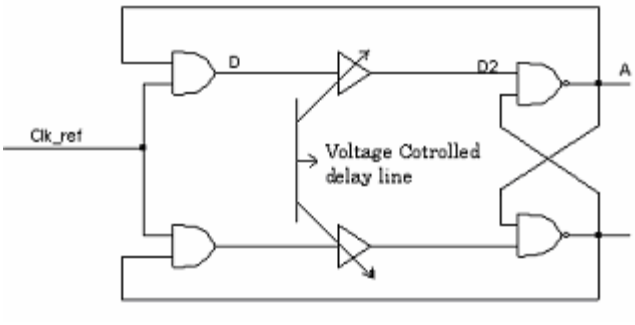

Fig. 3. The Delay Controlled Oscillator

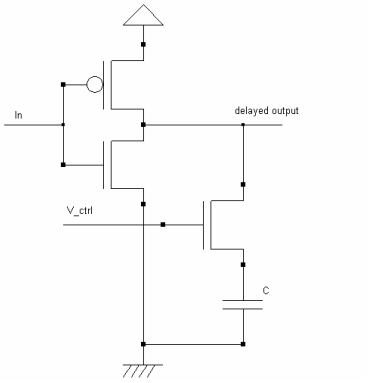

Fig. 4. Conventional delay cells used in the delay line.

can be used to generate high frequency clock signal. Reference clock is applied to the both input of the flip-flop. When the reference clock is low, the both outputs of the flip-flop are 'Hi'. If the reference clock *clk_ref* becomes 'Hi', *D* will also be 'Hi'. This signal (*D*) will arrive at point *D2*, *A* will become 'Lo'. But the output *B* will still remain 'Hi'. As the input of the AND gate *A* becomes 'Lo', the output *D* will turn to 'Lo'. When this low value will appear at the input (*D2)* of the NAND gate, the output *A* again turns on (as at this time the other input *B* of the NAND gate is 'Hi'). Thus the output at *A* will toggle as long as the clk_ref is 'Hi' and the toggling frequency will depends on the delay of the AND and NAND gate.

2.3 Delay-controlled flip-flop

The toggling frequency can be controlled by placing a delay line between point *D* and *D2*. The schematic of the flip-flop with delay line is shown in fig. 3. The toggling frequency depends on the value of the delay line. If the output of the flip-flop *A* changes from 'Hi' to 'Lo' (vice versa) and when this changed value reaches at *D2,* the output *A* will again changes its state from 'Lo' to 'Hi' (vice versa). To generate a clock of 1 GHz clock frequency, this 'Hi' must exist for 0.5 ns. We have to make an arrangement so that the changed signal at *D* must arrive at point *D2* after T_{delay}= (0.5ns-$T_{delay\text{-}AND}$ - $T_{delay\text{-}NAND}$). So we place a delay line which will generate a delay equal to T_{delay}. Then the output will toggle at 1 GHz frequency. By changing the delay of the delay line, it is possible to generate clock of other frequencies.

2.4 Voltage Controlled Delay line

We have used a conventional voltage-controlled capacitor-loaded inverter delay line [9] to generate the desired delay. Fig. 4. shows a basic delay cell used in the delay lines. The accuracy of the clock generator largely depends on the precise delay of this delay cell. The delay line is constructed using conventional CMOS inverter. This type of delay element has lower power consumption than the differential pair delay element [10]. To improve the power supply noise rejection, regulated supply is used for the inverters of the delay line. An NMOS is connected between the output of the inverter and capacitor. The output of the loop filter is passed to the voltage regulator and then the output voltage V_{CTRL} is applied to the gate of NMOS which controls the delay of the cell by controlling charging and discharging current through the capacitor.

2.5 Delay Controller

Fig. 5. shows the delay controller used in the clock generator to adjust the delay of the delay cells when the delay is higher than the required. The output of this delay controller is connected to a charge pump. This delay controller is a phase detector [9] whose output is proportional to the phase difference of the invert of reference clock and signal at point *A* of the delay-controlled oscillator. Short pulses will be produced (*DN*) when the loop is locked to avoid the dead zone

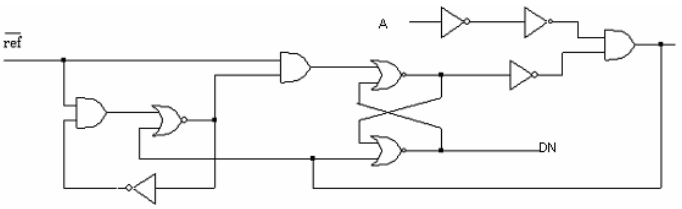

Fig. 5. Delay Controller.

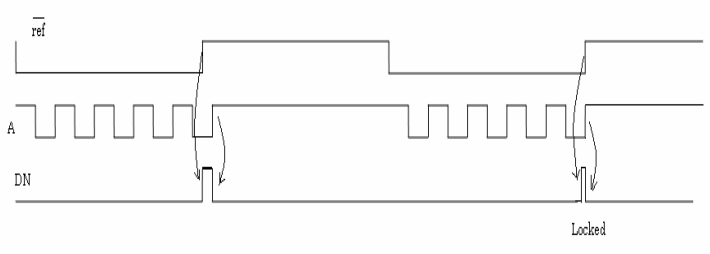

Fig. 6. Waveform during the locking process.

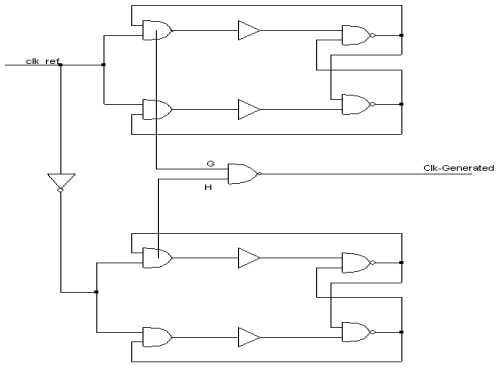

Fig. 7. The complete Delay Controlled Oscillator

[9]. Fig. 6. shows the waveforms during the locking process with the delay controller.

3 System Implementation

The schematic of fig. 7 shows the complete delay controlled oscillator. The first part will operate when the reference clock is 'Hi' and the lower flip-flop will work when the reference clock is 'Lo'. When the upper flip-flop will oscillate, the lower flip-flop will remain quit and its output will stay at 'Hi' (vice versa). Then the two outputs are nand-ed to get the final output. The output of the generated clock is shown in fig. 9. Fig. 8. shows the CMOS implementation of the oscillator. One thing to notice that that the two input of the NAND gate is taken from the point G and H so that the delay (skew) between the output and the reference clock remains minimum. The clock multiplier principle is illustrated on the timing diagram on fig. 9. The output from point *A* and the inverted *ref_clk* is fed to the phase detector (delay controller). The output of the PD is applied to the charge pump. The regulated output voltage V_{CTRL} is applied to the delay line embedded inside the level sensitive flip-flop. The delay of the delay line is changed according to the V_{CTRL} and the frequency of the generated clock is adjusted.

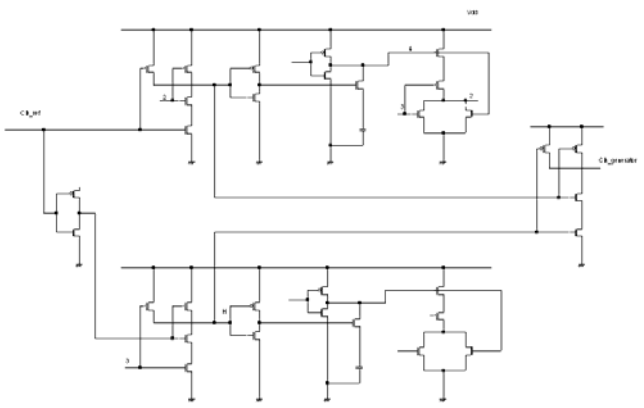

Fig. 8. CMOS Schematic of the Delay Controlled Oscillator.

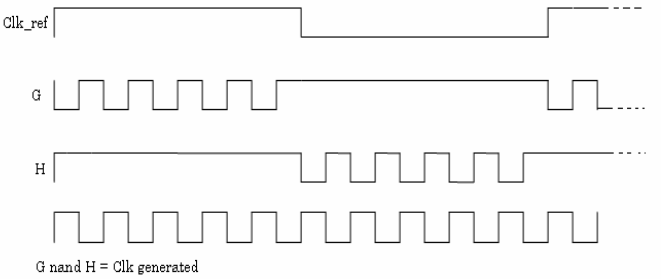

Fig. 9. Time diagram of the clock frequency multiplier

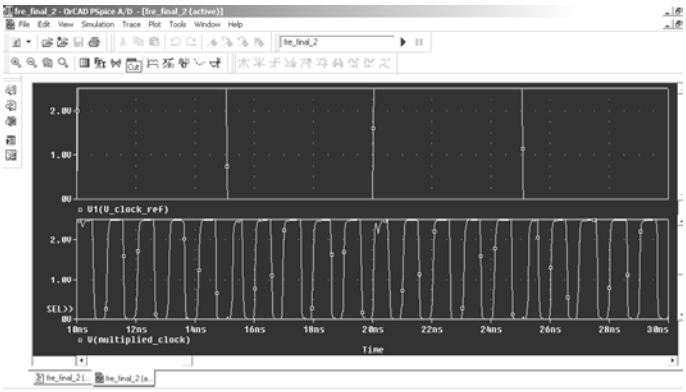

Fig. 10. Generated 1 GHz clock (lower plot) from 100MHz reference clock (upper plot)

4 Experiment Results

The clock frequency multiplier has been designed in a 0.25µm CMOS technology. The functionality of the multiplier is tested in PSPICE. We have used BSIM3v3 parameters to model the MOSFET in .25µm technology. The conventional Level 3 MOSFET model is not acceptable for submicron geometries. Shorter channel length requires considering subthreshold current modeling, channel width correction and many other important factors. The BSIM3v3 model circumvents many of the difficulties associated with Level 3 model. To improve simulation accuracy, we have used BSIM3v3 parameters for 0.25µm CMOS process. Fig. 10 shows the PSPICE simulation output of 1 GHz generated clock

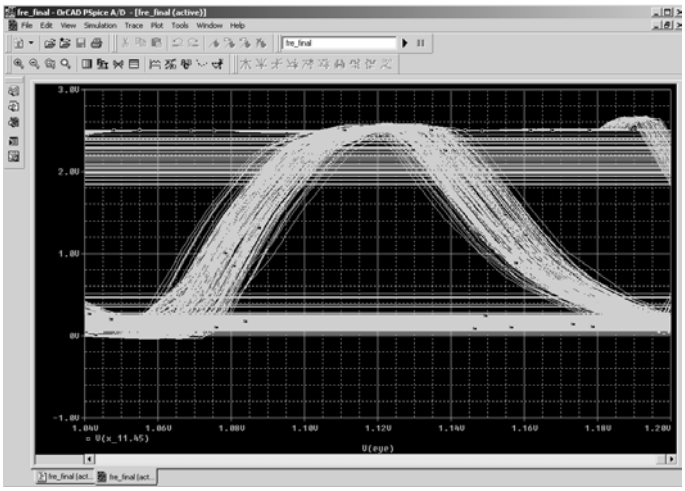

Fig. 10. Measured peak-to-peak cycle jitter

TABLE I
Summary of performance of Clock Generator

Process	0 .25µm CMOS technology.
Power supply	2.5 volt
Operating frequency range	10-500MHz
Output clock rate	20MHz-1GHz
Peak-to-peak jitter	82 ps @ 1 GHz
Power dissipation	0.822mW

from 100MHz reference clock. Power consumption is measured from PSPICE when the output clock is 1 GHz. As shown in fig. 11, the measured peak-to-peak jitter is 82 ps with a quit power supply when the output frequency is 1 GHz. Power consumption is measured in PSPICE which is 0.822mw for the delay-controlled oscillator and delay controller when the output frequency is 1 GHz with 10 MHz input reference clock. The result is the lowest that has been reported previously. Performance characteristics of the implemented clock generator is summarized in the Table I.

5 Conclusions

A DLL based high frequency clock generator has been proposed to achieve low jitter, low power clock in 0.25µm CMOS technology. The uses of DLL, delay controller and regulated power supply for the delay cells robust the jitter performance. The simulation of the proposed clock multiplier is performed using BSIM3v3 model parameters for in 0.25µm CMOS process which improves the simulation accuracy. This clock generator has a large range of input reference signal resulting a maximum of 1 GHz output clock with acceptable jitter.

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